UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,276	01/14/2002	Goro Nakatani	040894-5755	4701

9629 7590 08/08/2007

MORGAN LEWIS & BOCKIUS LLP
1111 PENNSYLVANIA AVENUE NW
WASHINGTON, DC 20004

EXAMINER	
IM, JUNGHWA M	
ART UNIT	**PAPER NUMBER**
2811	

MAIL DATE	DELIVERY MODE
08/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/043,276	NAKATANI ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 8-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 8-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 18, 2007 has been entered.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1 and 8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 1 and 8 recite the limitation "wherein said metal interconnect layer is an uppermost interconnect layer having a thickness capable of protecting the first interconnect layer and a device region of the semiconductor device." Note that the instant invention does not disclose this aspect that the uppermost metal layer has a thickness capable of protecting the first interconnect layer and a device region of the semiconductor device.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 8 recite the limitation "wherein said metal interconnect layer is an uppermost interconnect layer having a thickness capable of protecting the first interconnect layer and a device region of the semiconductor device." It is confusing to understand how the uppermost metal layer can protect the device region of the semiconductor device and the interconnect layer (other metal layer).. Furthermore, Fig 1 of the instant invention does not show a configuration that indicates an uppermost interconnect layer protects the first interconnect layer and a device region of the semiconductor device.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 8 and 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Loboda et al. (US 5818071), hereinafter Loboda in view of Braeckelmann et al. (US 6218302), hereinafter Braeckelmann.

Regarding claim 1, insofar as understood, Fig. 1 of Loboda shows semiconductor device comprising:

a first interconnect layer (3) arranged above a substrate on which a functional semiconductor region (2) is formed;

a silicon nitride film (5) a metal interconnect layer (7) said metal interconnect layer being consist of gold material (col. 1, line 59), wherein said metal interconnect layer is an uppermost interconnect layer having a thickness capable of protecting the first interconnect layer and a device region of the semiconductor device; and

a planarized polyimide (9) which is directly on the a silicon nitride film and surrounding the metal interconnect layer.

Fig. 1 of Loboda shows most aspect of the instant invention except an inter layer dielectric and the polyimide layer is removed at a part of a region of the metal interconnect layer and a bond wire is connected to the region of the metal interconnect layer. Fig. 11 of Braeckelmann shows that an inter layer dielectric (22) and a silicon nitride film (23) formed so as to cover entirely a top surface of said interlayer dielectric, covering over said silicon nitride film covering a surface of the first interconnect layer and the polyimide layer is removed at a part of a region of the metal interconnect layer and a bond wire (1104) is connected to the region of the metal interconnect layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Loboda to the device of Braeckelmann in order to have an additional inter layer dielectric layer under the silicon nitride layer for structural strength and the polyimide layer removed at a part of a region of the metal interconnect layer for wire connection.

Regarding claim 3, Braeckelmann discloses that the silicon nitride film is deposited by plasma deposit (col. 3, lines 49-51).

In addition, "high-density plasma CVD" is a process designation, and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp,* 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 8, insofar as understood, Fig. 1 of Loboda shows a semiconductor device comprising:

a first interconnect layer (5) covering a first portion of a surface of a functional semiconductor region (2);

a silicon nitride film (5) around the contacting hole on the surface of the first interconnect layer;

a barrier layer (8) covering the contacting hole and a portion of a surface of the silicon nitride film around the contacting hole, thereby forming a barrier layer region (col. 3, lines 65-68);

a metal interconnect region (7) consist of gold material (col. 7, lines 23-26) covering over the barrier region, thereby forming a metal interconnect region, wherein said metal interconnect layer is an uppermost interconnect layer having a thickness capable of protecting the first interconnect layer and a device region of the semiconductor device; and

a planarized polyimide (9) covering the metal interconnect layer and the silicon nitride surface around the metal interconnect region.

Fig. 1 of Loboda shows most aspect of the instant invention except an inter layer dielectric and that a portion of the polyimide layer is removed. Fig. 11 of Braeckelmann shows

an inter layer dielectric and silicon nitride covering a top surface of said inter layer dielectric an inter layer dielectric covering a second portion of the surface of the functional semiconductor region and a portion of a surface of said first interconnect layer, thereby forming a contacting hole on the surface of the first interconnect layer and the polyimide layer is removed at a part of a region of the metal interconnect layer and a bond wire (1104) is connected to the region of the metal interconnect layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Loboda to the device of Braeckelmann in order to have an additional inter layer dielectric layer under the silicon nitride layer for structural strength and the polyimide layer removed at a part of a region of the metal interconnect layer for wire connection.

Regarding claims 10 and 11, Braeckelmann discloses the first interconnect layer consists of aluminum (col. 3, lines 25-26).

Regarding claim 12, Braeckelmann discloses the inter layer dielectric consists of USG film (col. 3, lines 47-49).

Regarding claim 13, Fig. 11 of Braeckelmann shows the functional semiconductor region further comprises a polysilicon gate (108; col.2, lines 57-58) isolated from the first interconnect layer by a third dielectric layer (110), wherein the first interconnect layer is connected to the polysilicon gate through a contacting area (116) disposed within the second dielectric layer.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Loboda and Braeckelmann as applied to claim 8 above, and further in view of Toyosawa et al. (US 6441467), hereinafter Toyosawa.

Regarding claim 9, the combined teachings of Loboda and Braeckelmann shows substantially the entire claimed structure except "the barrier layer consists of titanium." Toyosawa discloses that the barrier layer consists of titanium (col. 7, lines 48-50).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Toyosawa to the device of Braeckelmann in order to have the barrier layer consisted of titanium to diffusion of the metallic compound to the neighboring layer while using the well-known barrier material.

Response to Arguments

Applicant's arguments filed May 18, 2007 have been fully considered but they are not persuasive. The rejection stands, modified only to accommodate the amendments made to the claims by Applicant. New rejections are made in response to Applicant's amended claims. In addition, the examiner presents the remarks below in response to Applicant's arguments.

As discussed in the office action above, the amended portion is not disclosed in the instant invention. Therefore, it is confusing to understand how a thickness of the uppermost metal layer could be able to protect the structure underneath, in particular, a device region of the semiconductor device. Note that the uppermost metal layer of the instant invention is a thin gold interconnect, and one of ordinary skill in the art would understand that the gold interconnect is not designed for the protection of the underlying structures, in particular, other metal interconnect and the device region.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Junghwa M. Im
Examiner
Art Unit 2811

jmi
8/2/2007